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Design and verification of an FPGA programmable logic element based on Sense-Switch pFLASH

Key words: Field programmable gate array (FPGA); Programmable logic element (PLE); Boolean logic operation; Look-up table; Sense-Switch pFLASH; Threshold voltage

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Motivation

1. From the realization of FPGA process classification, there are three types, i.e., SRAM-based FPGA, anti-fuse-based FPGA, and Flash-based FPGA.
2. The advantages of SRAM-based FPGA are large scale and high computing power. The disadvantage is that data in configuration SRAM are lost after power-off, so non-volatile memory needs to be configured on the periphery, and the bitstream data will be loaded again during each power-on.
3. The advantages of anti-fuse-based FPGA include non-loss of data after power-off and excellent anti-radiation performance. The disadvantage is that the anti-fuse layout area used for programmable wiring switches is large, so the equivalent number of system gates achieved by this type of FPGA is smaller than 6 million.

4. Flash-based FPGA currently on the market is designed based on n-channel flash, so the radiation resistance performance is not very good, and each PLE can only realize the function of LUT3.

Main idea

1. With Flash technology of p-channel , Sense-Switch pFLASH (SSPF) was conducted.
2. A novel PLE based on SSPF and using COOL (choice of operational logic) technology is proposed for Flash-based FPGA.
3. All three-bit look-up table (LUT3) functions, partial four-bit look-up table (LUT4) functions, latch functions, and d flip flop (DFF) with enable and reset functions can be realized in each PLE.
4. To accurately control the threshold voltage after SSPF programming, the multistep programming method is adopted, and the threshold voltage is adjusted to the preset range after several programming sessions.

Method

1. SSPF is the most critical core technology for designing Flash-based FPGA. SSPF is composed of two p-type floating gate metal oxide semiconductor (MOS) transistors that share a floating gate (FG) and a control gate (CG).

T1 and T2 are a programming/erase transistor (Sense) and a switch transistor (Switch) for signal transmission control, respectively.

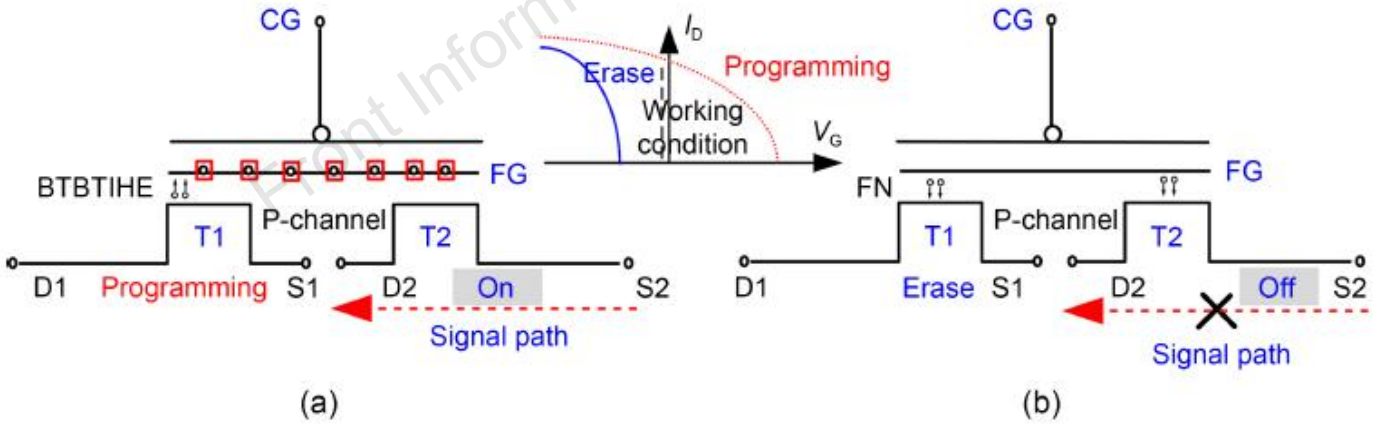
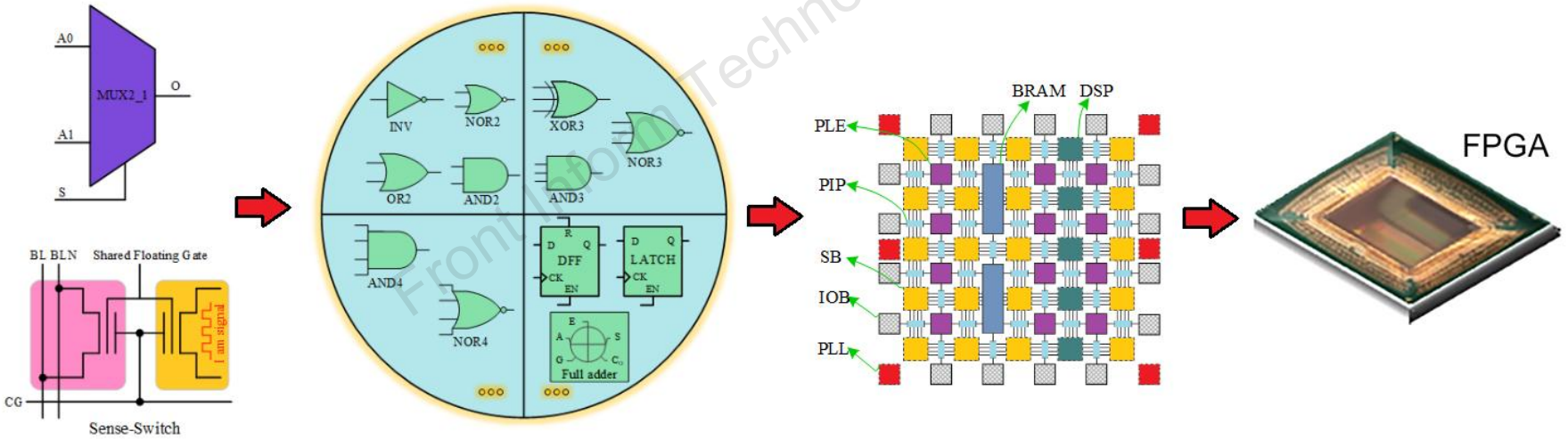


Fig. 2 Schematic diagram of the SSPF working mode: (a) "on" state (programming state); (b) "off" state (erase state) (SSPF: Sense-Switch pFLASH; CG: control gate; FG: floating gate; FN: Fowler–Nordheim; BTBTIHE: band-to-band tunneling induced hot electron)

Method (Cont'd)

2. The basic digital logic gates such as NAND2, NOR2, and INV can be realized by different ways of connecting the input of MUX2_1. By combining MUX2_1 with SSPF, more complex digital logic functions can be realized.



Method (Cont'd)

3. In order to realize the function of combinatorial logic operation (LUT3/LUT4) and sequential logic operation (DFF), the circuit of the PLE was designed in this study, which contains 4 MUX2_1, 36 SSPFs, 1 NOR2, and 13 NOT.

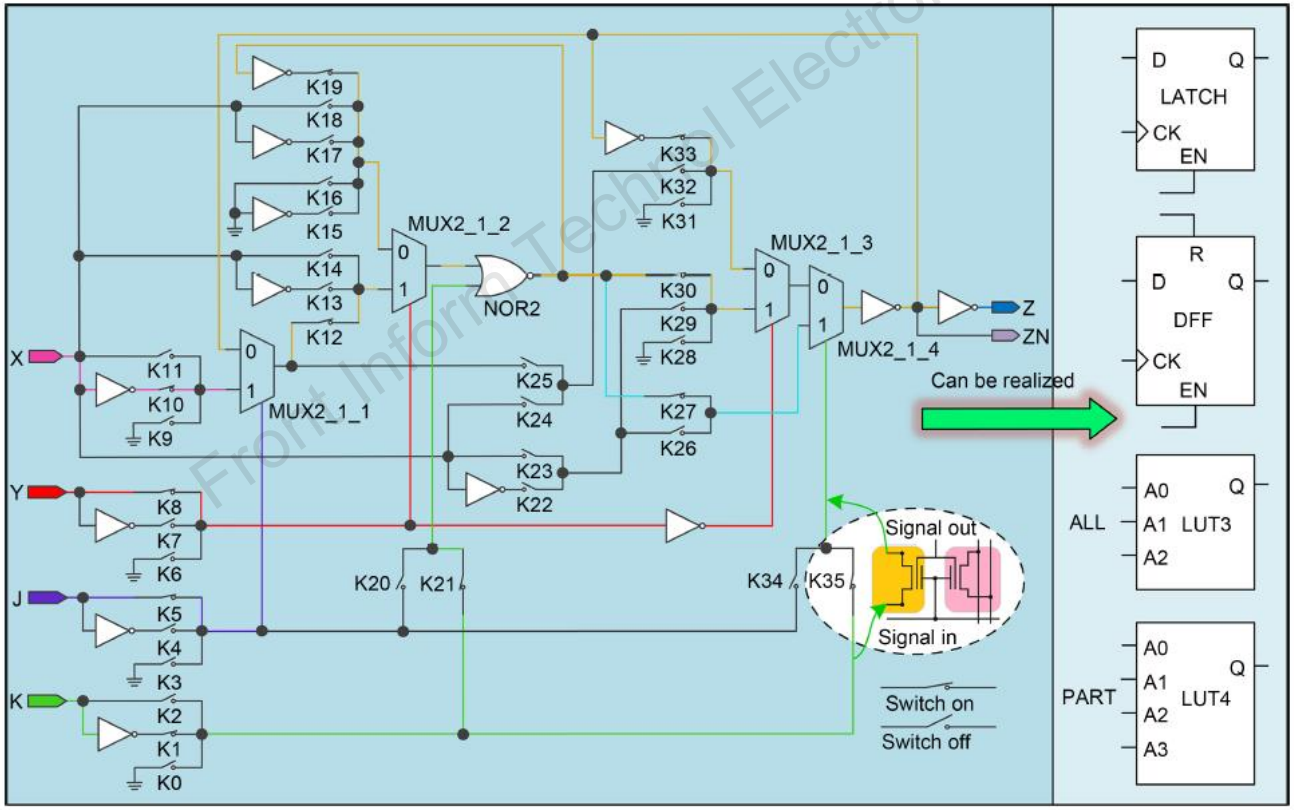


Fig. 6 Circuit diagram of the PLE designed in this study and the principle of implementing a DFF with enable and reset functions (PLE: programmable logic element; DFF: d flip flop)

Method (Cont'd)

4. In order to control the consistency of the SSPF switch delay parameters, a multistep programming method is used.

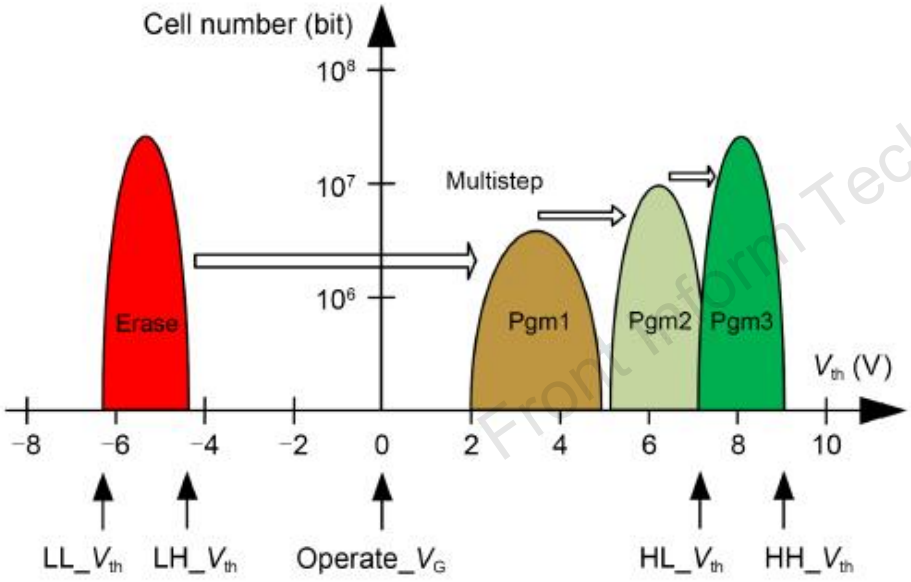


Fig. 18 Multistep programming (Pgm) approach

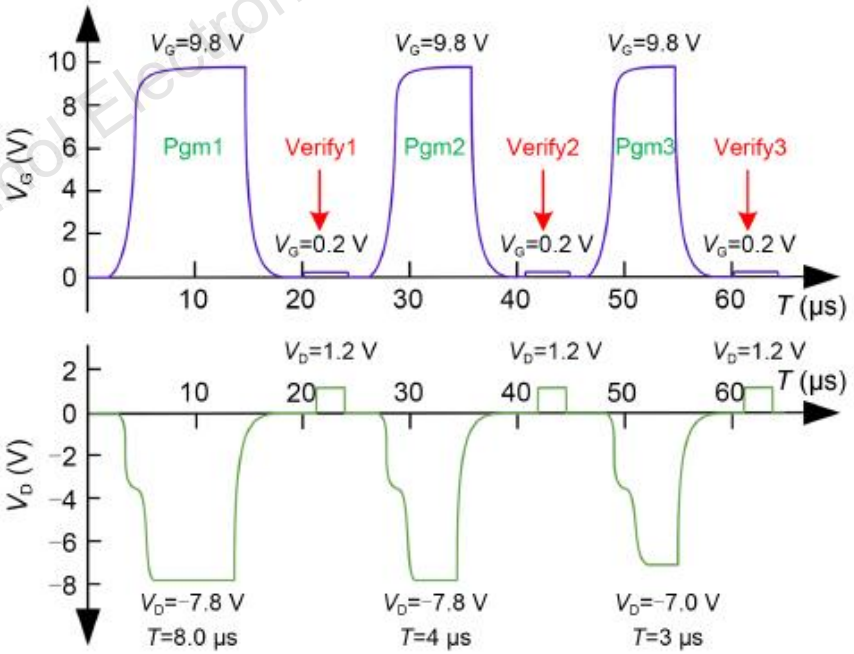


Fig. 20 A typical programming (Pgm) waveform

Method (Cont'd)

5. The design is verified by the actual circuit based on the 90 nm pFLASH process.

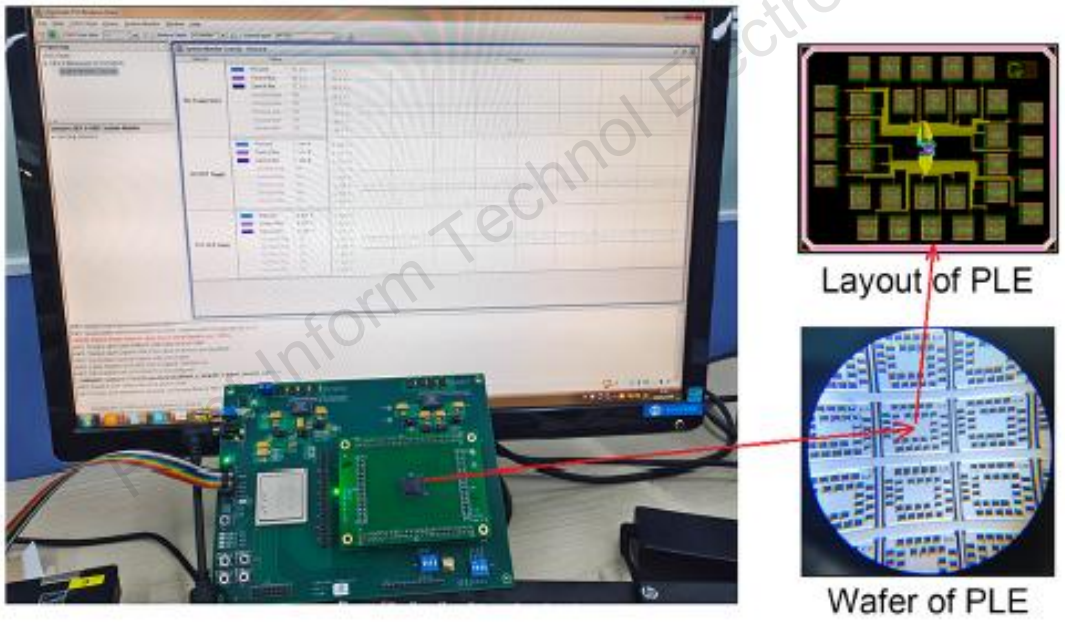
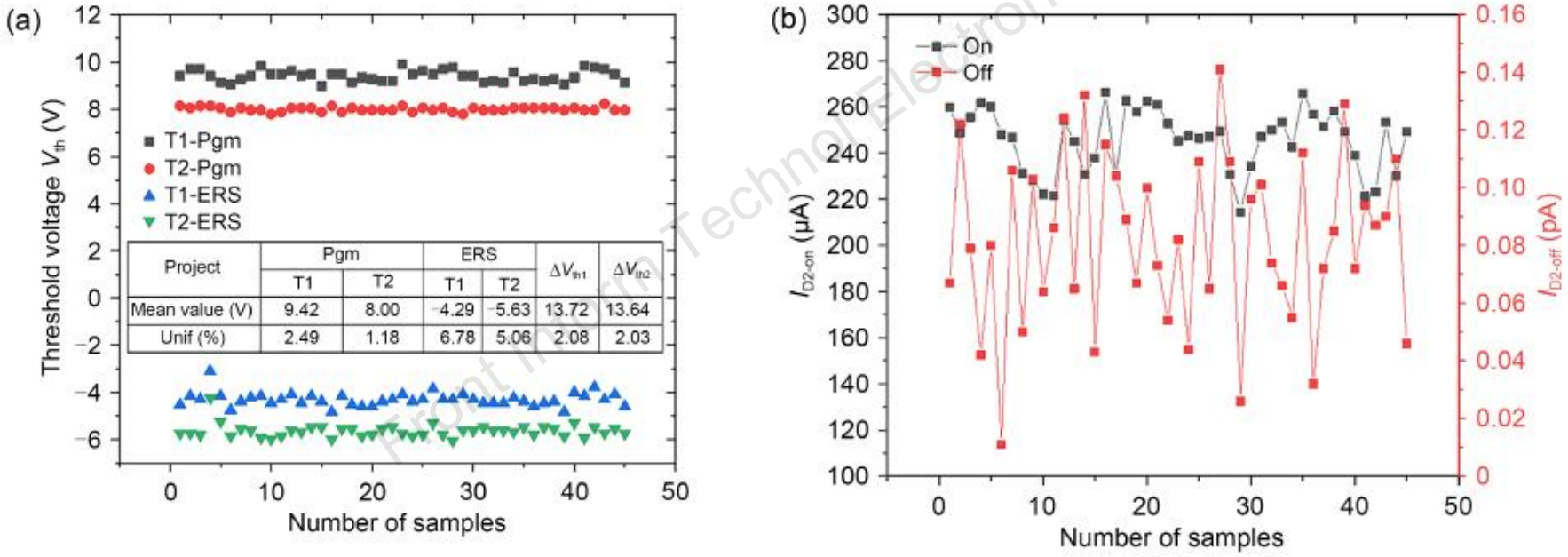


Fig. 21 Silicon wafer and test evaluation board of the programmable logic element (PLE)

Major results

The results of the SSPF test



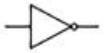
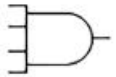
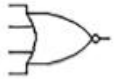
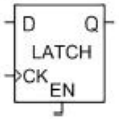
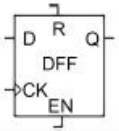
Project	Pgm		ERS		ΔV_{th1}	ΔV_{th2}
	T1	T2	T1	T2		
Mean value (V)	9.42	8.00	-4.29	-5.63	13.72	13.64
Unif (%)	2.49	1.18	6.78	5.06	2.08	2.03

Fig. 22 Characteristics of the SSPF: (a) T1 and T2 threshold voltage accumulation statistics; (b) cumulative statistics of the “on/off” states of the transistor T2 (SSPF: Sense-Switch pFLASH; Pgm: programming; ERS: erase; Unif: uniformity)

Major results (Cont'd)

Test results of PLE at three temperatures

Table 4 Test results of PLE at three temperatures

Function	Symbol	Delay (ns)		
		−55 °C	25 °C	125 °C
INV		0.44	0.47	0.51
AND2		0.52	0.56	0.59
NOR2		0.53	0.57	0.62
AND3		0.66	0.69	0.73
NOR3		0.72	0.77	0.83
XOR3		0.88	0.91	0.98
AND4		0.85	0.88	0.95
NOR4		0.85	0.89	0.96
LATCH		0.96	1.01	1.08
DFF		0.59	0.65	0.71

PLE: programmable logic element; DFF: d flip flop

Conclusions

1. With the 90 nm pFLASH process technology, a PLE was designed and manufactured.

2. With 4 MUX2_1, 36 SSPFs, 1 NOR2, and 13 NOT in each PLE, all LUT3 functions, partial LUT4 functions, latch functions, and DFF with enable and reset functions can be realized.

3. By measuring Sense-Switch pFLASH and PLE circuits, the results show that the programmable function of PLE works normally. The delay of the typical combinatorial logic operation AND3 is 0.69 ns, and the delay of the sequential logic operation DFF is 0.65 ns.

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